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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, DANNY	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 03/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/967,177	BERGH ET AL.	
	Examiner	Art Unit	
	Danny Nguyen	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-6, 9-13, 17-20, 23-25, 27, 28, 34-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Morron et al (USPN 6,025,980).

Regarding claims 1, 3, Morron et al disclose control circuit for an electrical relay (e.g. see fig. 1, 5 and 6), the circuit comprises a solid state switch (Q1 shown in fig 6) is coupled to a relay operator (L1) to control energization of the relay operator; and a leakage current suppression circuit (e.g. comparator 15 shown in fig. 1) configured to be coupled electrically in parallel with the solid state to place the switch in a conducting state and thereby to energize the relay operator when a control signal current level is above a leakage current threshold, and to place the switch in a non-conducting state and thereby to de-energize the relay operator when the control signal level is below a leakage current threshold (e.g. col. 2, lines 38-45, col. 3, 4, lines 47-3, and lines 32-35).

Regarding claim 2, Morron et al disclose the solid state switch (Q1) and the leakage current suppression circuit (15) are coupled to a DC bus (e.g. bus 8 shown in fig. 1), and the solid state switch is configured to be coupled in series with the relay operator (shown in fig. 6).

Regarding claims 4 and 23, Morron et al disclose a rectifier circuit (such as a full wave rectifier 29) for converting alternating current signals to direct current control signals.

Regarding claims 5, 6, 24, 25, 37, Morron et al disclose a signal conditioning circuit (e.g. regulator circuit 30 and capacitors C6 and C7 shown in fig. 1 and 7) for smoothing the direct current control signal and limiting the voltage of the direct current control signals to desired level.

Regarding claims 9, 10,17, 18, 27, 28, Morron et al disclose the leakage current suppression circuit includes a pair of resistors in series (e.g. series resistors Rmax and R2) about a node (e.g. the base of transistor Q1), and wherein the leakage current suppression circuit is operative to place the solid state switch (Q1) in a conducting state when a voltage at the node is above a desired level (e.g. col. 2, lines 39-44).

Regarding claims 11, 19, 20, 23, Morron et al disclose a control circuit for an electrical relay (fig. 1), the circuit comprises a rectifier circuit (a full wave rectifier 29) for receiving AC control signals and for outputting DC control signals; a DC bus (such as bus 56 or 57) coupled to the rectifier circuit for receiving the DC control signals; a control signal conditioning circuit (e.g. regulator 30) coupled to the DC bus for conditioning the DC control signals; a solid state switch (Q1 shown in fig 6) is coupled to a relay operator (L1)to control energization of the relay operator; and a leakage current suppression circuit (e.g. comparator 15 shown in fig. 1) configured to be coupled electrically in parallel with the solid state to place the switch in a conducting state and thereby to energize the relay operator when a control signal current level is above a

leakage current threshold, and to place the switch in a non-conducting state and thereby to de-energize the relay operator when the control signal level is below a leakage current threshold (e.g. col. 2, lines 38-45, col. 3, 4, lines 47-3, and lines 32-35).

Regarding claims 12 and 13, Morron et al disclose the control signal conditioning circuit includes a capacitor (e.g. C6 shown in fig. 7) for smoothing the DC signals.

Regarding claim 34, Morron et al disclose a method for controlling a relay circuit, the method comprises controlling a conductive state of a solid state switch (Q1) in series with a relay coil (L1) such that the relay coil is energized if a current level of an input control signal is above a predetermined leakage current threshold level and is deenergized if the current level of the input control signal is below a predetermined leakage current threshold level (e.g. see fig. 1, 5 and 6, and col. 3, 4, lines 64-3 and lines 32-35).

Regarding claim 35, Morron et al disclose the solid state switch is disposed electrically in parallel with a leakage current suppression circuit (15) having a pair of resistors (e.g. resistor Rmax and R2) and a node (such as the base of the transistor Q1), and wherein the conductive state of the solid state switch is controlled based upon voltage at the node to regulate energization of the coil (col. 3, 4, lines 64-3).

Regarding claim 36, Morron et al disclose the voltage at the node is applied to a base of the solid state switch, and wherein current applied to the base of the solid state switch is limited (by resistor 24).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 7, 8, 15, 16, 26, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morron et al in view of Misencik (USPN 5,541,800). Morron et al disclose all limitations of claims 1, 11, 19, and 34 except for having LED indicator. Misencik discloses a ground fault interrupt circuit comprises a LED indicator (col. 2, lines 8-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the protection circuit of Morron et al with the LED indicator as taught by Misencik in order to provide indication that a leakage current error has occurred (e.g. col. 2, lines 57-60).

3. Claims 29, 30, 32, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gernhardt et al (USPN 5,864,455) in view of Morron et al. Gernhardt et al disclose terminal block relay assembly (such as fig. 1) comprises a terminal block including input terminals (26 and 28), output terminals (38 and 40), a bay (such recess 98) for receiving a relay (16), and connections (304 and 314) for routing signals between the terminals and the relay; a relay disposed in the bay and coupled to the connections, the relay having an operator (19); a circuit board (14) supported in the terminal block and coupled to the input terminals and to the relay operator via two of the connections (via conductors 30 and 36 and 42 and 44), but Misencik does not disclose the leakage current protection as claimed. Morron et al disclose a solid state switch (Q1 shown in fig

6) is coupled to a relay operator (L1) to control energization of the relay operator; and a leakage current suppression circuit (e.g. comparator 15 shown in fig. 1) configured to be coupled electrically in parallel with the solid state to place the switch in a conducting state and thereby to energize the relay operator when a control signal current level is above a leakage current threshold, and to place the switch in a non-conducting state and thereby to de-energize the relay operator when the control signal level is below a leakage current threshold (e.g. col. 2, lines 38-45, col. 3, 4, lines 47-3, and lines 32-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the protection circuit of Misencik et al with the the protection circuit as taught by Morron et al because Morron et al teaches that the earth leakage protection circuit for use with both circuit breakers and relays within both 50 Hz and 60 HZ electrical distribution circuits with the same or higher degree of harmonic attenuation of the harmonics within the associated electrical circuit, without substantial increase in circuit component cost (col. 1, lines 42-48).

4. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gerhardt et al in view of Morron et al and further in view of Misencik (USPN 5,541,800). Gerhardt and Morron disclose all limitations of claim 29 except for having LED indicator. Misencik discloses a ground fault interrupt circuit comprises a LED indicator (col. 2, lines 8-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the protection circuit of Gerhardt and Morron with the LED indicator as taught by Misencik in order to provide indication that a leakage current error has occurred (e.g. col. 2, lines 57-60).

5. Claim 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morron et al in view of Gerhardt et al. Morron et al disclose all limitations of claim 19 except for the relay and the switch are supported as claimed. Gerhardt et al disclose a leakage current protector (fig. 1 and fig. 10) comprises the relay (16) and the switch (e.g. 232) are supported on the circuit board (14) and on a terminal block (e.g. terminal block shown in fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the elements of protection circuit of Morron with the circuit board as taught by Gerhardt et al in order to protect elements against damage.

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morron et al in view of Obreartuin (USPN 6,275,400). Morron et al disclose all limitations of claim 11 except for having a diode as claimed. Obreartuin discloses a circuit comprises a diode (Z1) for clamping voltage at the desired level. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the protection circuit of Morron with the clamping diode as taught by OBreartuin in order to clamp the DC voltage from the rectifier at the desired control level (col. 1, lines 56-59).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (571)-272-2054. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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3/4/2004

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